REMARKS

In the outstanding Final Office Action, the Examiner objected to the drawings for failing to comply with 37 C.F.R. § 1.84 (p)(5); objected to the specification for various informalities; objected to the specification for failing to provide proper antecedent basis in claims 3-5 and 38-39; objected to the drawings under 37 C.F.R. § 1.83(a) for failing to show every feature of the claims; objected to claims 1, 2 and 39, for various informalities; rejected claims 1-5 and 34-39 under 35 U.S.C. § 112, second paragraph for being indefinite; rejected claims 1, 2, 35 and 36 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,306,940 to Yamazaki ("Yamazaki"); and rejected claims 1-5 and 34-39 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,087,706 to Dawson et al. ("Dawson").

By this amendment, Applicants amend claims 1-4 and 35-39. Claims 1-5 and 34-39 remain pending.

Objections to the Drawings

Objections under 37 C.F.R. § 1.84(p)(5)

The Examiner objected to the drawings as failing to comply with 37 C.F.R. § 1.84(p)(5), for including reference characters not included in the specification. Specifically, the Examiner objects to reference character "21" in Figure 4A as not being included in the specification. The Examiner further objected to the specification for specifically referencing the monocrystalline silicon substrate as reference character "41" at page 32 line 3. Accordingly, Applicants have amended the specification at page 32, line 3 to replace reference character "41" with reference character 21.

Objections under 37 C.F.R. § 1.83(a)

The Examiner further objected to the drawings under 37 C.F.R. § 1.83(a) for failing to show every feature of the claimed invention. This objection coincides with the objection to the specification for failing to provide proper antecedent basis for the claimed subject matter. These two objections will be discussed together below.

Objections to the Specification

The Examiner first objected to the specification for various informalities. Applicants have corrected the specification at pages 31-31 and 61-62, as indicated in the above Amendment to the Specification section of this paper.

Additionally the Examiner objected to the specification for failing to provide proper antecedent basis for the claimed subject matter, and, for similar reasons, objected to the drawings for failing to show every feature of the claimed invention. Although Applicants do not necessarily agree with the Examiner's characterization of the specification and drawings[1], Applicants have amended claims 3-4 and 38-39 to address the Examiner's concerns.

For example, claims 3, 38 and 39, as amended, recite a combination including, "said gate insulating film is formed on a top surface and sides of the semiconductor layer in said element regions which are not covered with said element isolating insulating film." Applicants respectfully submit that this element is clearly shown in, for example, Figures 17B, 19B, and 19C, wherein gate insulating film 73 is formed on the top and sides of semiconductor layer 71 in element regions not covered with the

[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicants decline to automatically subscribe to any statement of characterization in the Office Action.

element isolating insulating film 72, wherein the gate electrode 74 is formed on the gate insulating film 73. *See also* Applicants' specification at, for example, page 62, line 16 - page 63, line 21.

With respect to claim 5, however, the Examiner appears to assert that the language "the difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating element is substantially at least a junction depth of said source/drain region," as recited in claim 5, is not described in the specification, or shown in the drawings. Applicants respectfully disagree.

Applicants respectfully submit that the specification indeed provides support for claim 5. The specification describes the relationship between "the step amount δ, and the threshold voltage V_{th} for MOS transistors of different junction depths x_j." Applicants' specification, page 58, lines 5-11. Moreover, corresponding Figure 15 shows a series of curves for different junction depths x_j including points wherein the step amount δ is substantially the same as the junction depth x_j, thereby providing exemplary support for the claimed "the difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating element is substantially at least a junction depth of said source/drain region," as recited in claim 5. Accordingly, Applicants respectfully request the objections to the drawings and the specification be withdrawn.

Objections to the Claims

The Examiner objected to claims 1, 2, and 39 for failing to provide proper antecedent basis. Specifically the Examiner stated:

> "[c]laim 1, line 8 the phrase 'the element regions' has no antecedent basis ... [c]laim 2, line 8, the phrase 'said element regions' has no antecedent basis ... [c]laim 39, line 2 the phrase 'the gate insulating film' has no antecedent basis." Office Action, page 4, lines 13-16.

With respect to claims 1 and 2, Applicants submit that claims 1 and 2 have been amended to recite a combination including at least, "element regions," thus providing proper antecedent basis.

With respect to claim 39, which depends from claim 2, Applicants submit that claim 2 has been further amended to include a recitation of "a gate insulating film," thus providing proper antecedent basis for "the gate insulating film" recited in claim 39. Accordingly, Applicants respectfully request that the objections to claims 1, 2, and 39 be withdrawn.

Rejection under 35 U.S.C. § 112, second paragraph

The Examiner rejected claims 1-5 and 34-39 under 35 U.S.C. § 112, second paragraph, as being indefinite. Specifically, the Examiner appears to assert that the phrase "an element isolating film provided in the trench for partitioning said semiconductor layer into an element region," as recited in claims 1-3, is vague and indefinite. Accordingly, Applicants have amended claims 1-3 to recite a combination including, "an element isolating film provided in the trench for partitioning said semiconductor layer into a plurality of element regions." Thus, Applicants respectfully request the rejection of claims 1-5 and 34-39 under 35 U.S.C. § 112, second paragraph, be withdrawn.

Rejections under 35 U.S.C. §§ 102(b), 102(e)

Regarding the rejection of claims 1-2 and 35-36 under 35 U.S.C. § 102(b) as being anticipated by Yamazaki, and claims 1-5 and 34-39 under 35 U.S.C. § 102(e) as

being anticipated by Dawson, Applicants respectfully disagree with the Examiner's arguments and conclusions as set forth in the outstanding Office Action. Accordingly, Applicants respectfully traverse these rejections.

In order to properly anticipate Applicants' claimed invention under 35 U.S.C. §102, each and every element of the claim in issue must be found, "either expressly or inherently described, in a single prior art reference." "The identical invention must be shown in as complete detail as is contained in the . . . claim. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." *See* M.P.E.P. § 2131, (8th ed., 2001).

Yamazaki

Applicants respectfully traverse the Examiner's rejection of claims 1-2 and 35-36 under 35 U.S.C. § 102(b) as being anticipated by Yamazaki. Claim 1, for example, is not anticipated by Yamazaki because the reference fails to teach each and every element of the claim. In particular, Yamazaki at least fails to teach the claimed combination including "a difference in height from the substrate between the top surface position of said element isolating insulating film and the top surface position of said semiconductor layer is at least three times as large as the thickness of said gate insulating film," as recited in claim 1.

The Examiner contends that Yamazaki teaches "a trench (the area occupied by the lower portion of the oxide film [110])." Office Action at pages 5 and 10. Element 110 in Yamazaki is a field oxide (col. 14, lines 65-67), however, and the lower portion of which does not constitute a trench. A silicon nitride film (not shown) is first formed on the epitaxial layer 103. This silicon nitride film is partially removed, and the oxide film 110 is formed on the epitaxial layer 103 using a LOCOS process. Yamazaki, col. 10,

lines 53-55. Contrary to the Examiner's assertion, the bottom of film 110 is not a trench. Since the oxide layer 110 is formed on the epitaxial layer, and subsequently into the epitaxial layer, no part of the epitaxial layer is removed to form a trench of any kind. On the other hand, Yamazaki clearly identifies element 112 as a "trench." See, for example, col. 15, lines 2-7. If the lower portion of field oxide film 110 were a trench, Yamazaki would have disclosed it as such. Furthermore, Yamazaki specifically uses LOCOS to provide isolation, and does not use shallow trench isolation, thus any film that could provide element isolation would not be found in trench 112. Claim 1, therefore, is distinguishable over Yamazaki at least for this reason.

Applicants note that trenches 112 of Yamazaki include a BPSG film 115c, which might be argued to correspond to the claimed "element isolating insulating film" (see Fig. 8C, col. 15, lines 2-7). BPSG film 115c, however, does not extend above a surface of epitaxial layer 103 between trenches 112 (see Fig. 8c). Accordingly, Yamazaki does not teach the claimed combination including "a difference in height from the substrate between the top surface position of said element isolating insulating film and the top surface position of said semiconductor layer is at least three times as large as the thickness of said gate insulating film," and claim 1 is distinguishable over Yamazaki for this reason as well.

Claim 2, while of different scope, recites limitations similar to those recited in claim 1. Claim 2 is therefore distinguishable over Yamazaki for reasons discussed above in regard to claim 1.

In light of the above-described deficiencies of Yamazaki, Applicants submit that claims 1 and 2 are allowable over the applied reference, and claims 35 and 36 are allowable at least due to their dependence from claims 1 and 2, respectively.

Dawson

Applicants respectfully traverse the Examiner's rejection of claims 1-5 and 34-39 under 35 U.S.C. § 102(e) as being anticipated by Dawson. Claim 1, for example, is not anticipated by Dawson because the reference fails to teach each and every element of the claim. In particular, Dawson at least fails to teach the claimed combination including "an element isolating insulating film," as recited in claim 1.

The Examiner apparently contends that trench fill material 80 and dielectric layer 5 of Dawson correspond to the claimed "element isolating insulating film", as recited in claim 1. Trench fill material 80 does not extend above the surface of substrate 10 (see Dawson, Fig. 4G), and thus cannot constitute the claimed element isolating insulating film such that "a difference in height from the substrate between the top surface position of said element isolating insulating film and the top surface position of said semiconductor layer is at least three times as large as the thickness of said gate insulating film," as recited in claim 1.

The Examiner also contends that Dawson teaches a "trench (the area occupied by the lower portion of the dielectric film [5] and the dielectric film [80])." Office Action at page 7. To the extent the Examiner's position is understood, Applicants note that Fig. 4H clearly shows that the lower portion of dielectric layer 5 does not extend over element 14, which Dawson clearly discloses as a "trench region," delineated by dashed lines in Figs. 4B-4H. Col. 5, lines 52-54, for example. Applicants respectfully submit, therefore, that the Examiner has improperly associated the lower portion of dielectric

layer 5 with part of trench 14, when there is no teaching in Dawson as such. If Dawson intended to include dielectric layer 5 in trench 14, the reference would have shown dashed lines in Fig. 4H extending over dielectric layer 5. Accordingly, dielectric layer 5 also does not correspond to the claimed element isolating insulating film because it is not "provided in the trench," as recited in claim 1.

Moreover, Dawson teaches the formation of isolation regions 15 (see Figure 2) using known LOCOS techniques to isolate active areas 70. Dawson, col. 6, lines 5-12. Dawson also teaches forming trenches 14 (see Figures 4B-4H) in semiconductor layer 10 which provides partial isolation for active areas 70. Dawson, col. 5, lines 63-65. Trenches 14 are filled with trench fill material 80, and after trench fill material is etched to a level below semiconductor layer 10, planar dielectric layer 5 is formed over portions of active areas 70 and trench fill material 80. Contact holes 2 are subsequently formed in planar dielectric layer 5. Dielectric layer 5 and trench fill material 80 are separated from one another by contact plugs 6 formed in contact holes 2, and thus also do not collectively constitute the claimed "element isolating insulating film", as recited in claim 1, since contact plugs 6 are necessarily conductive and are neither isolating nor insulating.

Even if the combination of trench fill material 80 and dielectric layer 5 could be reasonably construed as Applicants' "element isolating insulating film," as recited in claim 1, Applicants submit that Dawson still would fail to teach each and every element of the claim. For example, Dawson fails to teach the claimed combination including "the top surface position of said element isolating insulating film is not higher than a top surface position of the gate electrode," as recited in amended claim 1. The alleged

element isolating insulating film composed of trench fill material 80 and dielectric layer 5 extends to a position that is far above the top surface of gate electrode 30. Therefore, the Examiner's current characterization of Dawson fails to teach the element "the top surface position of said element isolating insulating film is not higher than a top surface position of the gate electrode," as recited in amended claim 1.

For at least the foregoing reasons, Applicants submit that Dawson fails to teach each and every element of claim 1. Claims 2 and 3 recite limitations similar to those recited in claim 1, and are therefore distinguishable over claim Dawson for reason discussed above in regard to claim 1.

Thus, in view of the above-noted shortcomings of Dawson, claims 1-3 are allowable over the applied reference, and claims 4, 5, and 34-39 are allowable at least due to their corresponding dependence from claims 1-3.

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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